UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,828	07/15/2003	Yi-Ming Sheu	TSM03-0140	7191

43859 7590 08/04/2005

SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER	
FARAHANI, DANA	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/619,828	SHEU ET AL.
	Examiner	Art Unit
	Dana Farahani	2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/27/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Doyle et al., hereinafter Doyle (US Patent Application Publication 2002/0074598A1), previously cited.

Regarding claim 1, Doyle discloses in figure 7 a transistor device comprising a semiconductor region having a top surface, a source region 58 in the semiconductor region; a drain region 60 in the semiconductor region; a channel region in the semiconductor region between the source region and the drain region (not shown but inherent to the structure); an impurity region 56 within the channel region and spaced from the top surface, the impurity region laterally spaced from the source and drain regions, as can be seen in the figure; a gate 62 overlying the channel region; and a gate dielectric (not shown, but inherent to the gate 62) between the gate and the channel region.

Regarding claim 3, see paragraph 48, line 11, wherein it is implied that the semiconductor region is silicon.

Regarding claim 6, see paragraph 36, wherein it is stated that oxygen ions may also be implanted into the semiconductor region.

Regarding claim 7, see paragraph 35, line 5, wherein it is stated that the channel region comprises a strained channel region.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle in view of Shaw et al., hereinafter Shaw (US Patent 4,069,094), previously cited.

Doyle discloses the limitations in the claim, as discussed above, but does not disclose the semiconductor region is monocrystalline silicon.

Shaw teaches monocrystalline silicon has advantages over polycrystalline silicon since it is more uniformed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use monocrystalline silicon in the structure of the Doyle reference to take advantage of the properties associated with the material, such as uniformity and lower resistivity.

5. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle.

Regarding claim 4, Doyle substantially discloses the claimed invention, as discussed above, except for expressly disclosing the relative distances of the impurity region from the surface of the semiconductor region, and the source/drain regions from the surface.

Doyle teaches that the depth of the implantation of the impurities in the semiconductor region can be modified (see paragraph 37). Therefore, it would have been obvious to one of

ordinary skill in the art at the time of the invention to make modifications regarding the proximate distance of the impurity region from the top surface of the semiconductor region, to adjust the depth of the impurity region in accordance with the size of a given MOS transistor and the available fabrication techniques. Also, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 5, Doyle substantially discloses the claimed invention, as discussed above, except for expressly disclosing silicon dioxide being used in the gate dielectric. It would have been obvious to one of ordinary skill in the art at the time of the invention to use silicon dioxide in the gate dielectric, since it is well known that silicon dioxide is extensively used in the gate dielectric portions of the MOS transistors.

6. Claims 8 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle as applied to claim 1 above, and further in view of Sagarwala et al., hereinafter Sagarwala (US Patent 6,759,717), previously cited.

Regarding claim 8, Doyle discloses the limitations in the claim, as discussed above with respect to claim 1, but does not disclose sidewall spacers for the gate of the device and lightly doped portions in the source and the drain of the device.

Sagarwala discloses in figure 11, sidewall spacers 50 and 38; and lightly doped portions 56 of the source and drain regions shown in the figure. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the structure of the Sagarwala reference, commonly known as a LDD structure, to benefit from the advantages of these kind of

structures, such as reduced peak electric field at the edges of the source and drain regions (see Sagarwala, column 1, lines 44-47).

Regarding claims 9-12, Doyle discloses the limitations in the claims, as discussed above, but does not disclose a second transistor.

Sagarwala discloses second source/drain regions and a second gate, 44' and 20 respectively; a second channel region (not shown, but inherent to the device) between the second source and the second drain; and a second gate dielectric 24 all shown in figure 11. (Note that the second transistor could be a n channel transistor, in which case the transistor on the right side of the second transistor would be a p type transistor, as the conductivity types could be flipped). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the MOS transistor of the Doyle reference in a CMOS type structure, in order to make the MOS transistor structure of the Doyle reference usable in an integrated circuit structure that implements a CMOS type structure. CMOS type structures have advantages such as lower power consumption and smaller sizes over the traditional NMOS and PMOS transistors, and increasingly are used in modern integrated circuits.

Response to Arguments

7. Applicants' arguments filed 5/20/05 have been fully considered but they are not persuasive.

Applicants argue that the limitation of an impurity region laterally spaced from the source and drain regions are not met by the Doyle reference. Applicants argue that since the impurities of the reference are inserted through the mask shown in figures 5 and 6, therefore, the impurities

are located at the channel region. However, it is readily apparent from the reference that the impurities are scattered between the source and drain region, and therefore, they are laterally spaced from the source and drain.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

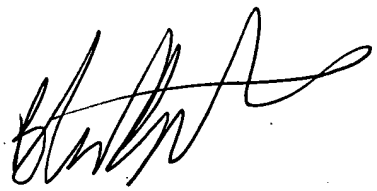
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722 The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani



B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER